REMARKS

The application has been reviewed in light of the Office Action mailed October 26, 2004. Reconsideration of the application is respectfully requested. Claims 59-66, 69, 70, 72, 78 and 83-85 have been amended, and new claims 132-157 have been added without adding new matter. Reconsideration of the application is requested in light of the foregoing amendments and the following remarks.

Claims 59-85 stand rejected under 35 U.S.C. § 103(a) as being unpatentable over Endoh et al., U.S. Patent No. 5,374,788 (hereinafter "Endoh") in view of Ball et al., U.S. Patent No. 6,246,112 (hereinafter "Ball"), Panicker, U.S. Patent No. 5,089,881 (hereinafter "Panicker"), and Carey, U.S. Patent No. 5,272,600 (hereinafter "Carey"). This rejection is respectfully traversed for the following reasons.

The present invention relates to a high performance chip carrier. The chip carrier has a substrate having at least one through-hole, and a multi-sheet layer which has conductive and insulating layers, and a signal wiring layer. The multi-sheet layer is formed over both sides of the substrate, and passes through the through-hole, such that an electrical connection can be made between chips mounted on opposite sides of the substrate. Additionally, the substrate may have active and/or passive circuit components formed thereon. The signal wiring layer may have signal lines electrically connecting with the circuit components formed on the substrate, and electrically connecting with chips mounted over the multi-sheet layer.

Claim 59 recites a processor system comprising a "substrate having a through-hole, ... [and] a multi-layer structure ... comprising: a conductive layer; a signal wiring layer, said conductive layer and said signal wiring layer having an insulating layer interposed between them." Further, claim 59 has been amended to recite an "interconnect wiring structure extending from said signal wiring layer through said insulating and conductive layers."

The cited references, taken alone or in combination, fail to teach or suggest the subject matter of claim 59. Endoh discloses a method for making a printed wiring board. Specifically, Endoh discloses an aluminum metal core 1, plated with a protective nickel layer 3, which in turn is covered by a metal oxide layer 4 and then by a non-conductive layer 5. The metal oxide layer 4 enhances the adhesive force between layer 5 and the metal core 1. The Endoh wiring board has a through-hole 2, and a wiring layer 6 formed in the through-hole 2 and over a portion of the non-conductive layer 5. Column 3, lines 7-46, and Figure 1.

Endoh fails to teach or suggest an "interconnect wiring structure extending from said signal wiring layer through said insulating and conductive layers." Endoh's wiring layer 6, compared to the claimed signal wiring layer by the Office Action, has no interconnect wiring structures extending through any of its layers. The other references cited by the Office Action – Ball, Panicker and Carey – do not relate to substrates having through-holes and multilayer structures, and add nothing to Endoh to remedy its deficiency with respect to amended claim 59.

Claim 59 is allowable for at least this reason. Claims 60-85 depend from claim 59 and incorporate every limitation of claim 59. Claims 60-85 are allowable for at least the same reasons as for allowance of claim 59, and also because the unique combinations recited in these dependent claims are neither taught nor suggested by the cited references, taken alone or in combination.

For example, with respect to dependent claims 70-72 and 85, the Office Action admits that the Endoh fails to teach that the "insulating layer comprises a second insulating layer formed over the conductive plane, a third insulating layer formed over the signal wiring layer, a second conducive plane formed over the third insulating layer, and a fourth insulating layer formed over the second conductive plane." Office Action, page 5. The Office Action asserts, however, that it would have been obvious "to incorporate a second, third, and fourth insulating layers and a signal wiring layer, since it has been held that mere

duplication of the essential working parts of a device involves only routine skill in the art." Id.

For the foregoing proposition of obviousness, the Office Action relies on St. Regis Paper Co. v. Bemis Co., 198 USPQ 8, 549 F.2d 833 (7th Cir. 1977). Initially, the St. Regis Paper court relied on whether or not certain limitations created a "synergistic combination" as the test for obviousness. Id. at 838-39. That approach was overruled in Republic Ind., Inc. v. Schlage Lock Co., 200 U.S.P.Q. 769, 592 F.2d 963, 970-72 (7th Cir. 1979). Thus, the Office Action reliance on St. Regis Paper is improper.

Moreover, in St. Regis Paper the court found obviousness where the patentee merely added multiple layers to a bag to make the bag stronger. This analysis is not analogous to the subject invention. Applicants' invention provides for multiple layers of insulative and conductive layers not to make the substrate stronger, but rather to provide greater functionality. For example, with reference to Figure 4 and accompanying text of the specification, the layers between the signal layer 31 and the substrate 17 enable the signal layer to communicate with components on the substrate 17 via interconnect wiring 62, and layers above the signal layer 31 enable the signal layer to communicate with devices on the other side of the signal layer via interconnect wiring 60. Thus, the Office Action's assertion that multiple layers of the claimed invention are "mere duplication of the essential working parts" is not correct. Of course, the invention is not limited to the disclosed embodiments.

New claims 132-157 has been added to round out the scope of protection afforded the invention. Independent claim 132 recites a "substrate ... having at least one through-hole and ... a multi-layer structure ... comprising at least one conductive layer and a signal wiring layer, said at least one conductive layer and said signal wiring layer having an insulating layer interposed between them." Claim 132 also recites that the "signal wiring layer has an interconnect wiring structure ... extending through said insulating and conductive layers." Claim 132 is allowable for at least the same reasons discussed above

with respect to claim 59. Claims 133-157 depend from claim 132 and should be allowable for at least the same reasons as claim 132.

Applicants are submitting herewith an Information Disclosure Statement (IDS) containing references cited during prosecution of a related patent application, serial no. 10/191,277. Applicants wish to address a reference, Hamzehdoost et al., U.S. Patent No. 5,689,091 ("Hamzehdoost"), which has been applied in a rejection in the 10/191,277 application. (The Hamzehdoost reference is already of record in the subject application). Please note that Hamzehdoost fails to teach or suggest "interconnect wiring structure extending from said signal wiring layer, through said insulating and conductive layers, to said substrate," as recited in amended claim 59. Rather, Hamzehdoost discloses bonding wires extending from bondable areas 34 to a die 38 on a substrate. The bonding wires are not "interconnect wir[es] ... extending ... through ... insulating and conductive layers, to [a] substrate."

Applicants also wish to note that in the Notice of References Cited that accompanies the subject Office Action, the "Name" listed for references E and F is incorrect. The IDS being submitted herewith contains the references with correct names. In view of the above amendments, Applicants believe the pending application is in condition for allowance. The Examiner is therefore respectfully requested to withdraw the outstanding rejections and pass the application to issue.

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Respectfully submitted,

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